

claims. Accordingly, claims 1-20 are pending in this application and are submitted for consideration.

Claims 2-20 were found to contain allowable subject matter and would be allowed if rewritten to overcome the rejections under 35 USC § 112 and to include all the limitations of the base claims and any intervening claims. Applicants submit that all rejects have been sufficiently addressed herein, and therefore, request that claims 2-20 be allowed.

Claims 1-6 were objected to in the Office Action for a number of cited informalities. Claims 1-6 are amended herein. Applicants submit that each objection is adequately addressed by the amendments. In particular, the Examiner's suggestions have been adapted to the subject matter of the claims and adopted. Accordingly, Applicants request that the objections be withdrawn.

Claims 1-20 were rejected under 35 USC § 112, second paragraph as being indefinite. Regarding claim 1, claim 1 has been amended to clarify the processing as cycles or processing and that the recitation is for a cycle of processing. Furthermore, "values" of an output of said replica circuit have been replaced by --voltages-- to further clarify the subject matter claim 1. Regarding claim 2, "cause an integral of" has been replaced by --resetting--, and the recitations of lines 10-22 have been clarified. Regarding claim 3, "said bias current" has been changed to --said second bias current-- and "said successively summed value" has been changed to --said value obtained by said successively summing--. Claims 4 and 5 have been amended similar to claim 3. Thus, Applicants submit that claims 1-20, as submitted herein, comply with all the

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requirements of 35 USC § 112. Accordingly, Applicants request that the rejection be withdrawn and claims 1-20 be allowed.

Claim 1 was rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 6,154,083 to Gaudet et al. (hereinafter, "Gaudet"). It was asserted in the Office Action that Gaudet's figure 2 and at column 4, lines 39-40, the elements of the claim 1 are described. In particular, it is asserted in the Office Action that Gaudet's DLL 108 corresponds to the evaluation circuit of claim 1, Gaudet's comparator DAC 110 corresponds to the comparator circuit of claim 1, and Gaudet's current mirrors 112 correspond to the bias adjustment circuit of claim 1. Applicants respectfully traverse the rejection and assert that claim 1 recites subject matter not shown nor described by Gaudet.

Claim 1 of the present invention recites a semiconductor integrated circuit. The circuit includes an adjusted circuit, a replica circuit of the adjusted circuit, an evaluation circuit, a comparator circuit, and a bias adjustment circuit. The adjusted circuit has a first bias current flowing, and a slew rate of the adjusted circuit is dependent on the first bias current. The replica circuit has a second bias current flowing therein, and a value of the second bias current is substantially equal to that of the first bias current. The evaluation circuit is configured to repeat a cycle of processing. The cycle of processing includes steps of:

(1) Resetting an output thereof.

(2) Obtaining a difference between first and second voltages at given times. The first voltage is one at an output of the replica circuit at a time when a first time interval has elapsed after a given voltage having been step-inputted to the replica

circuit. The second value is one at the output of the replica circuit at a time when a second time interval has elapsed after a voltage equal to the given voltage having been step-inputted to the replica circuit. The second time interval is different from the first time interval.

(3) Successively summing the differences.

The comparator circuit is for comparing a value obtained by the successively summing with a reference value. The bias adjustment circuit is for changing the second bias current according to a comparison result of the comparator circuit at each of the given times.

According to the claimed configuration, an evaluation circuit repeats the cycle of processing, which is completely different from the DLL logic 108 of Gaudet. In contrast to the claimed invention, in Fig. 2 of Gaudet, DLL logic 108 compares the desired delay amount and the precision delay amount and generates a digital control signal that corresponds to a difference between the desired delay amount and the precision delay amount. See claim 1, and column 5, lines 25-27.

Moreover, digital-to-analog converter 110 converts the digital control signal to the bias signal provided to the replica I/O cell 102 (claim 1, and column 5, lines 36-39). In contrast, the comparator circuit of the present invention compares a value obtained by the successively summing with a reference value. Thus, the comparator circuit of claim 1 is different from the digital-to-analog converter 110 of Gaudet.

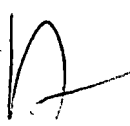
The current mirror circuit 112 of Gaudet responds to the bias signal by generating a plurality of bias current signals, wherein each of the bias current signals are provided to a corresponding one of the I/O cells of the integrated circuit to control

the delay through the corresponding I/O cell (claim 1, and column 5, lines 40-57). In contrast, the bias adjustment circuit of claim 1 changes the second bias current according to a comparison result of the comparator circuit at every said given times. Thus, the bias adjustment circuit of claim 1 is completely different from the current mirror circuit 112 of Gaudet.

Thus, Applicants submit that Gaudet fails to show or describe each and every element of claim 1. Accordingly, Applicants request that the rejection be withdrawn and claim be allowed.


In view of the above remarks, the Applicants respectfully submit that each of claims 1-20 recite subject matter which is neither disclosed nor suggested in the cited prior art. Applicants submit that this subject matter is more than sufficient to render the claimed invention unobvious to a person of ordinary skill in the art. Applicants therefore request that each of 1-20 be found allowable, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

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In the event this paper is not timely filed, the Applicants respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account No. 01-2300.

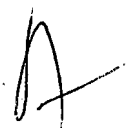
Respectfully submitted,



Brian A. Tollefson
Registration No. 46,338

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 Connecticut Avenue, N.W.,
Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-4810

BAT:tdd



MARKED UP COPY OF AMENDED CLAIMS

1. (Amended) A semiconductor integrated circuit comprising:

an adjusted circuit in which a first bias current flows, a slew rate of said adjusted circuit being dependent on said first bias current:

a replica circuit of said adjusted circuit in which a second bias current flows, a value of said second bias current being substantially equal to that of said first bias current;

an evaluation circuit configured to repeat a cycle of processing, said cycle of processing including:

resetting an output thereof;

obtaining a difference between first and second voltages [values of an output of said replica circuit] at given times, [said first and second values being respective ones at respective times when first and second time intervals has elapsed after a given value having been step-inputted to said replica circuit] said first voltage being one at an output of said replica circuit at a time when a first time interval has elapsed after a given voltage having been step-inputted to said replica circuit, said second value being one at said output of said replica circuit at a time when a second time interval has elapsed after a voltage equal to said given voltage having been step-inputted to said replica circuit, said second time interval being different from said first time interval; and

successively summing said differences;

a comparator circuit for comparing a value obtained by said successively summing with a reference value; and

a bias adjustment circuit for changing said second bias current according to a comparison result of said comparator circuit at every said given times.

2. (Amended) The semiconductor integrated circuit of claim 1, wherein said evaluation circuit comprises:

a subtraction/integration circuit integrating, as said successively summing, each difference between said first [output value] voltage and said second [output value] voltage; and

a control circuit;

wherein said control circuit is configured to repeat the steps of:

(1) [cause an integral of] resetting said subtraction/integration circuit [to be reset];

(2) repeating part of said cycle of processing at said given times, said part of said cycle of processing including:

[causing] resetting said replica circuit [to be reset];

next [causing said given value to be step-inputted] step-inputting said given voltage to said replica circuit;

[causing said output of said replica circuit as said first value to be provided] next providing said first voltage to said subtraction/integration circuit after or till said first time interval has elapsed from said step-inputting;

next [causing] resetting said replica circuit [to be reset];

next [said given value to be step-inputted] step-inputting said voltage equal to said given voltage to said replica circuit; and



[causing said output of said replica circuit as said second value to be provided] next providing said second voltage to said subtraction/integration circuit after or till said second time interval has elapsed from said previous step-inputting[; and repeat the processing of said (1) and (2)].

3. (Amended) The semiconductor integrated circuit of claim 2,
wherein said bias adjustment circuit is configured to step up said second bias current in response to judgment that a value obtained by said successively [summed value] summing is larger than said reference value by said comparator circuit,
wherein said control circuit is configured to cease [its] operation of said bias adjustment circuit in response to judgment that said value obtained by said successively [summed value] summing is smaller than said reference value.

4. (Amended) The semiconductor integrated circuit of claim 2,
wherein said bias adjustment circuit is configured to step down said second bias current in response to judgment that a value obtained by said successively [summed value] summing is smaller than said reference value by said comparator circuit, and
wherein said control circuit is configured to cease [its] operation of said bias adjustment circuit in response to judgment that said value obtained by said successively [summed value] summing is larger than said reference value.

5. (Amended) The semiconductor integrated circuit of claim 2,

wherein said bias adjustment circuit is configured to step down said second bias current in response to judgment that a value obtained by said successively [summed value] summing is smaller than said reference value by said comparator circuit, and step up said second bias current in response to judgment that said value obtained by said successively [summed value] summing is larger than said reference value by said comparator circuit,

wherein said control circuit is configured to cease [its] operation of said bias adjustment circuit in a case where an absolute value of a difference between said value obtained by said successively [summed value] summing and said reference value is smaller than a given value.

6. (Amended) The semiconductor integrated circuit of claim 3,

wherein said replica circuit has an inverting output and a non-inverting output,

wherein said subtraction/integration circuit comprises:

an operational amplifier circuit having an inverting input, a non-inverting input, an inverting output and a non-inverting output;

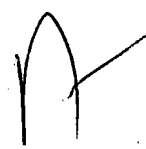
a first integrating capacitor connected between said inverting input and non-inverting output of said operational amplifier circuit;

a second integrating capacitor connected between said non-inverting input and inverting output of said operational amplifier circuit;

a reset switching circuit for resetting electric charges on said first and second integrating capacitors;

first and second sampling capacitors; and

a switching circuit for selectively charging said first and second sampling capacitors or said second and first sampling capacitors by said inverting output and non-inverting output, respectively, of said replica circuit, and thereafter transferring electric charges on said first and second sampling capacitors to said first and second integrating capacitors, respectively.

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